



Open SystemC Initiative (OSCI) Moving Up To The System-Level

European SystemC Users Group

DATE 2003

Agenda

- **Electronic Design: Moving Up To The System-Level**
 - A Brief Historical Perspective
- **OSCI: Mission, Developments & Silicon Success**
 - Why SystemC?
 - Mission: Model Concept to RTL
 - OSCI Development Update and Roadmap
 - Real World SystemC Silicon Success
 - Commercial Tool Momentum
 - University Research

The logo for SYSTEM C features the text "SYSTEM C" in a white, sans-serif font, centered within a dark blue, semi-circular shape. A white arc is positioned above the text. The logo is set against a background of horizontal lines that transition from yellow at the top to blue at the bottom.

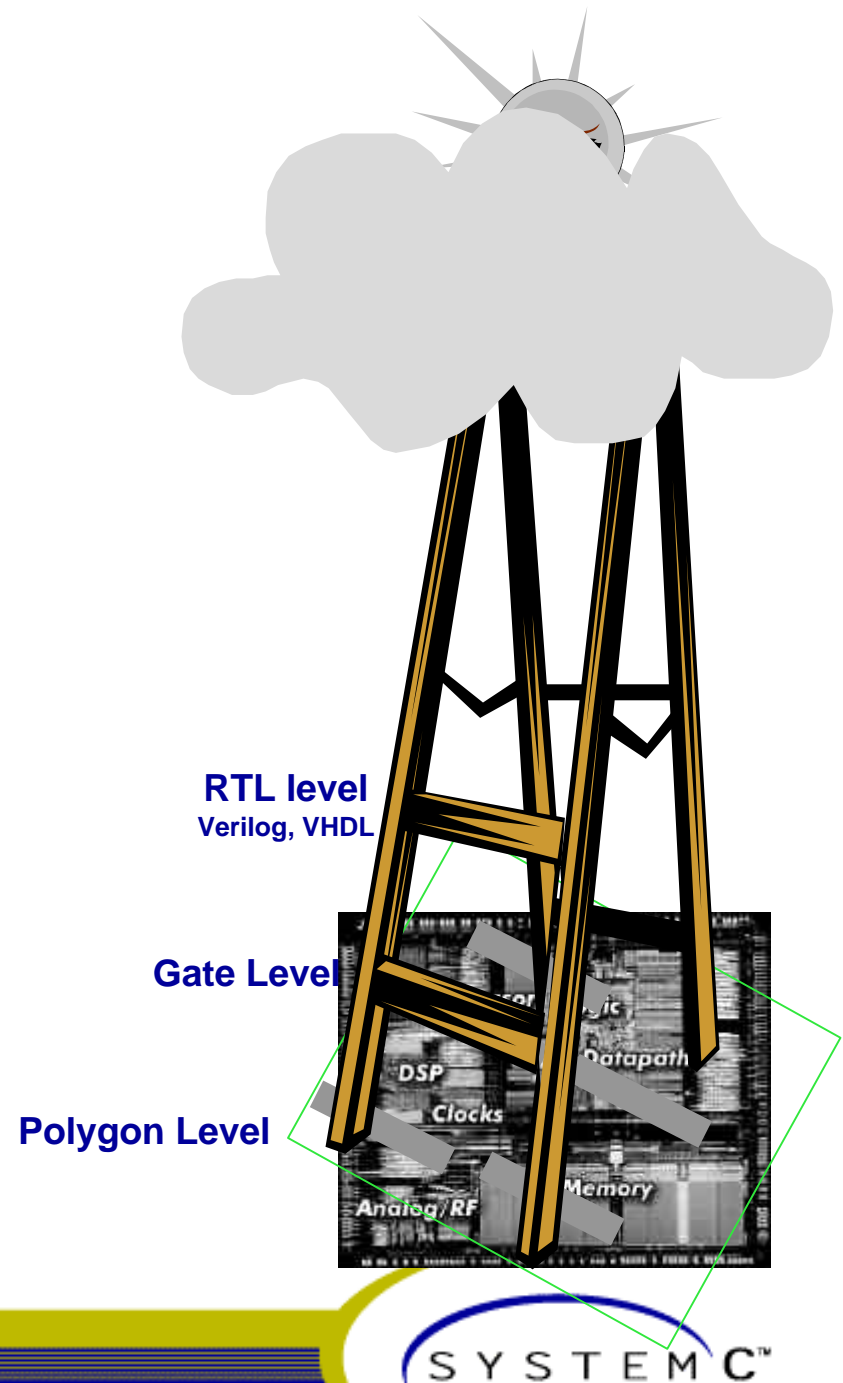
SYSTEM C™

Moving Up To The System- Level

A Brief Historical Perspective

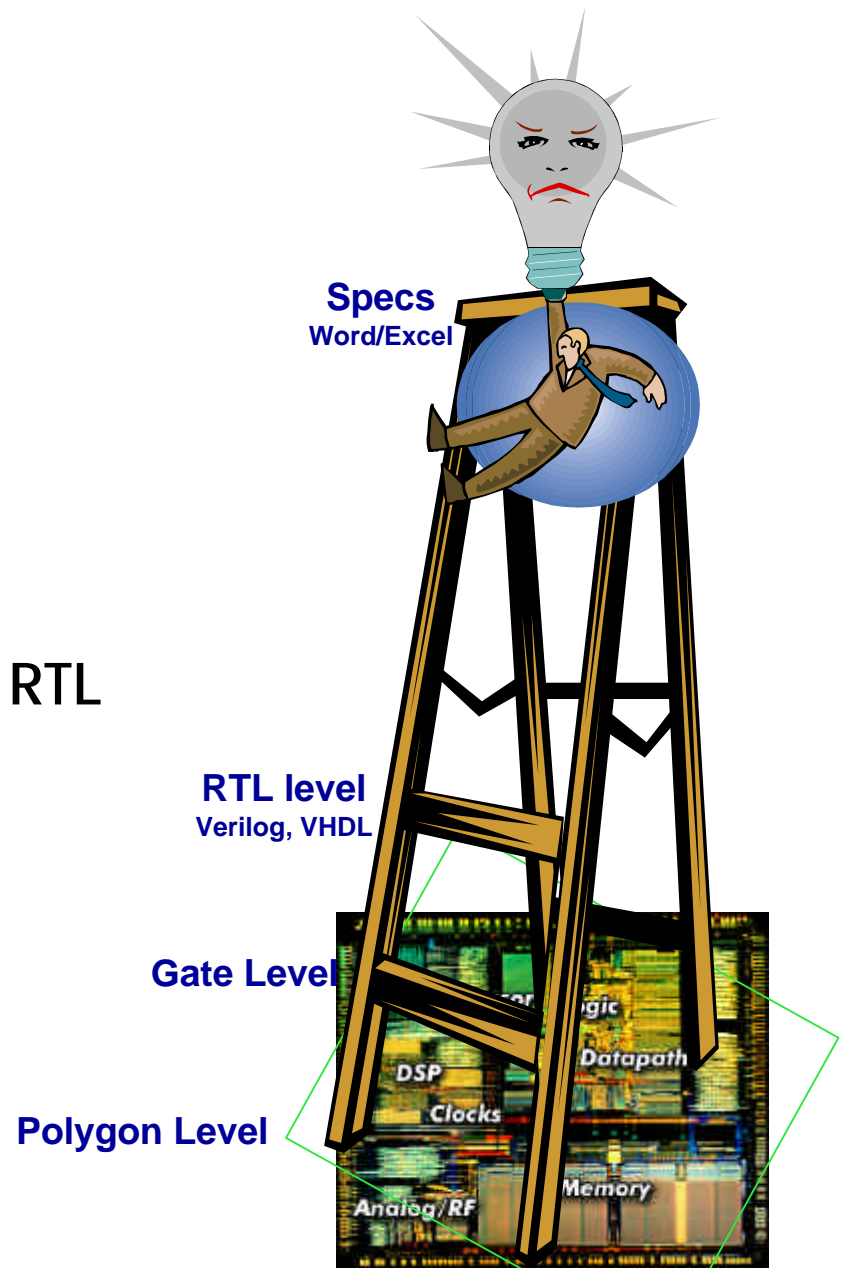
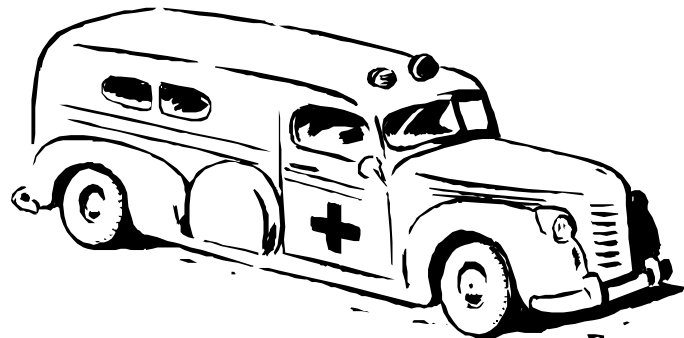
mid 70's to mid 90's

- Traditional bottom-up design replaced with HDL's top-down design approach
- Design abstraction moves upwards
- New levels of IP emerge
- EDA tools move up to enable path to silicon



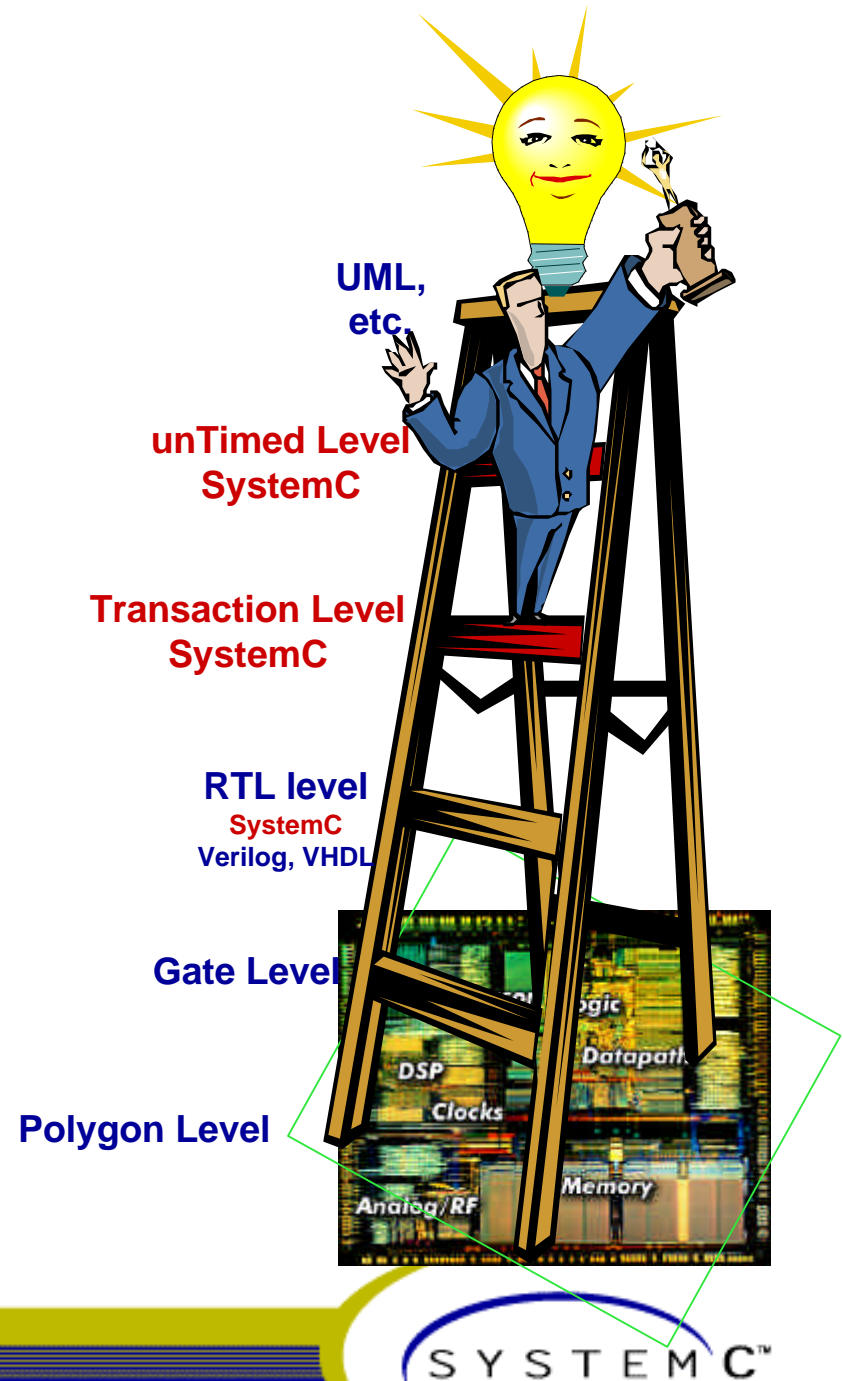
Mid 90's

- EDA confronted with:
 - System = software running on silicon!
 - Serious gap between system design & RTL

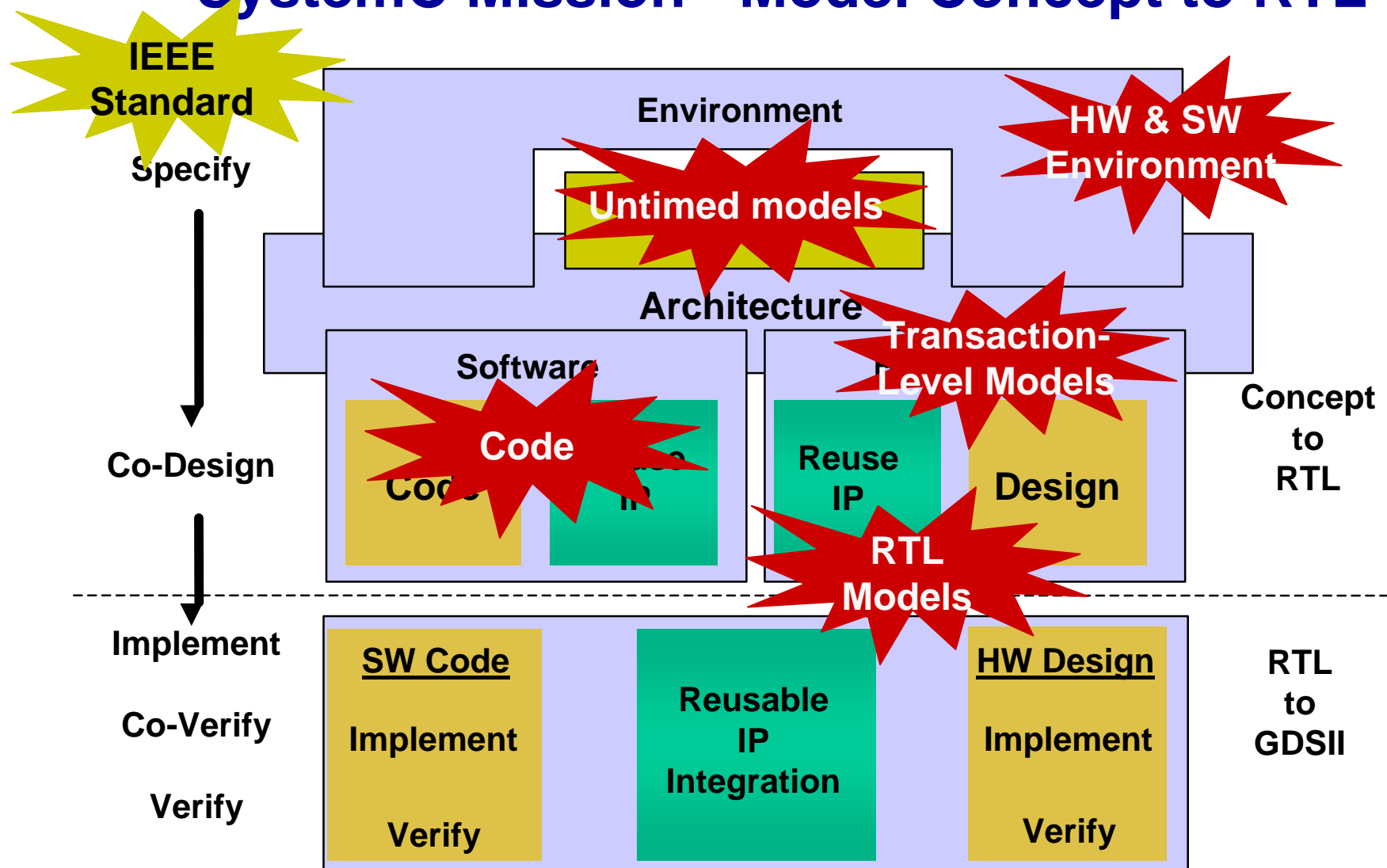


2002 & beyond

- Designs continue to move up to ever higher levels of abstraction
- SystemC bridges the gap with abstract modeling & RTL
- IP moves up, Again!
- EDA tools move up to ensure path to silicon

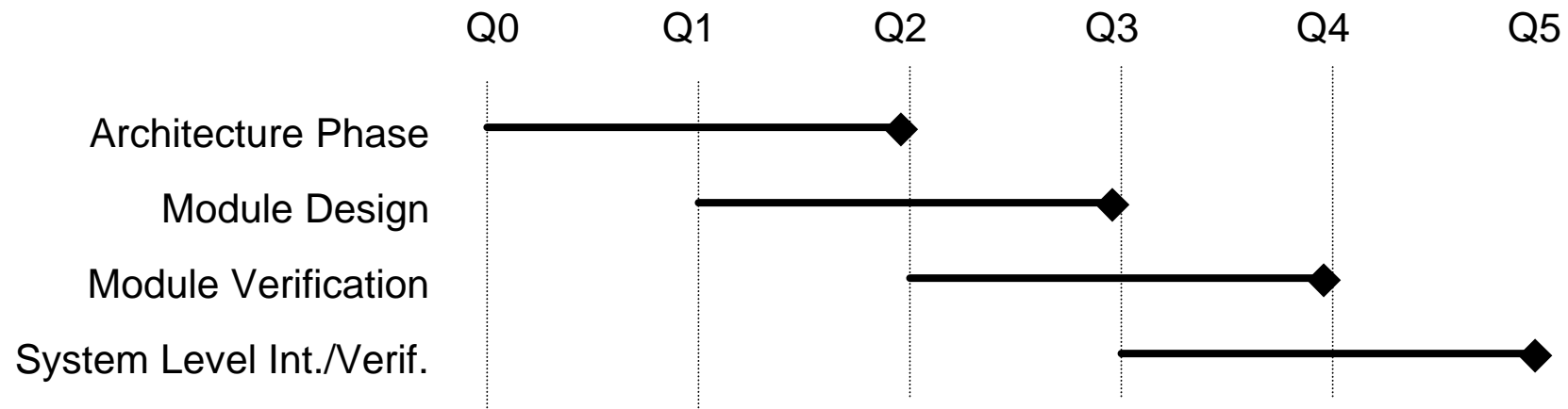


SystemC Mission - Model Concept to RTL



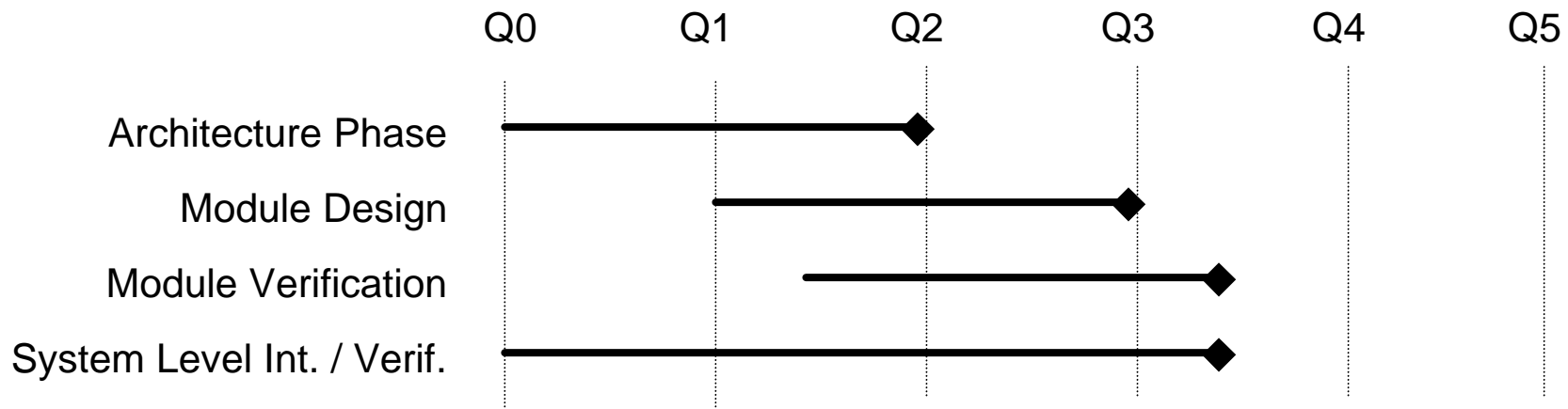
Traditional Design Flows

System Level Integration is always done last, is always on the critical path - and is always done too late for architectural redesign



Start at the System Level: Save Time / Money!

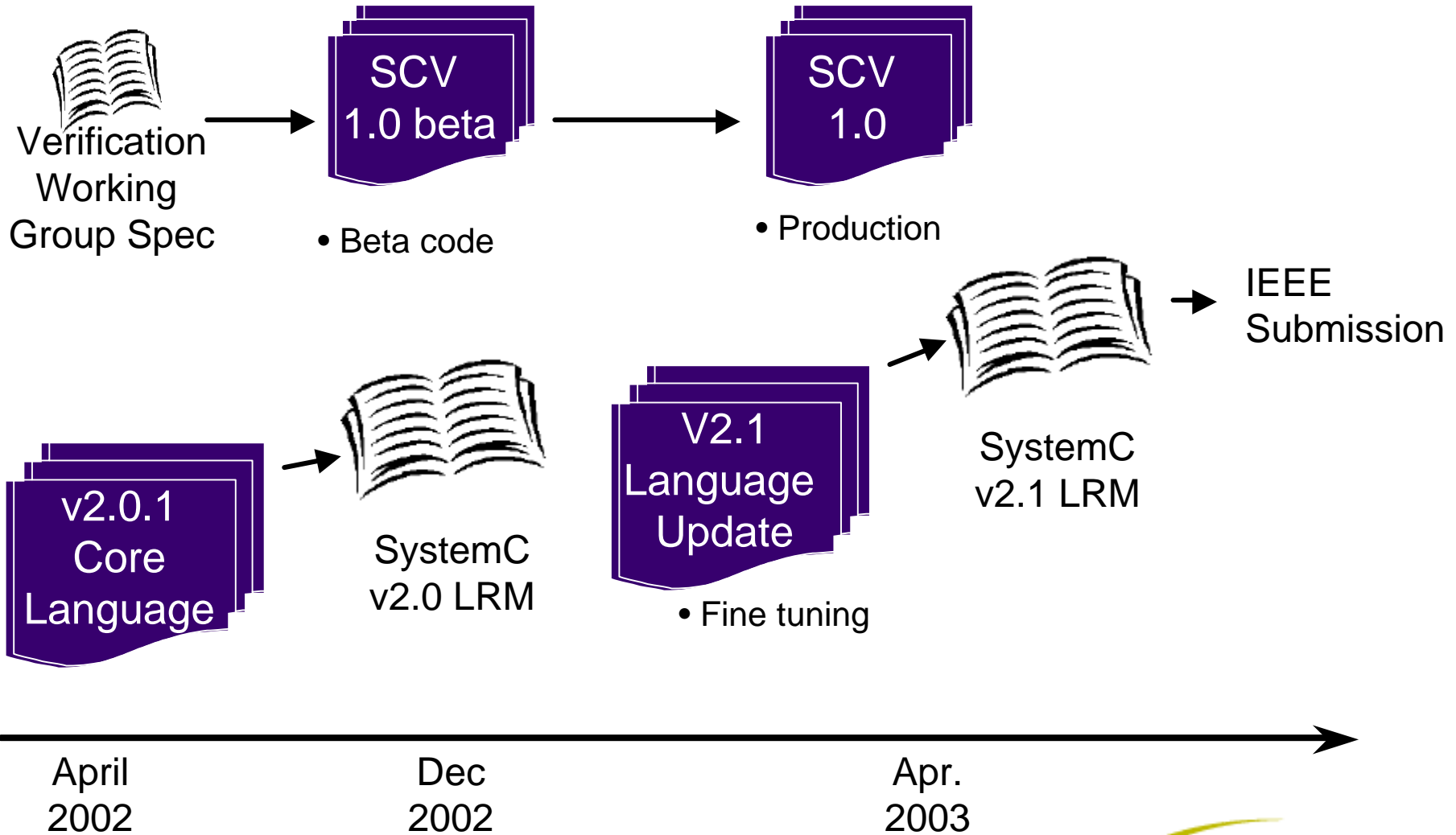
System Level Integration is done throughout the lifetime of the project



SystemC Development Highlights

- **Key OSCI Development Underway**
 - SCV-1.0 beta delivered
 - SystemC v2.1 underway
 - SystemC Synthesis working group formed
- **Driving for submission to the IEEE in 2003**
 - Complete LRM for SystemC v2.0 under review within OSCI
 - LRM for SystemC v2.1 => mid 2003
- **SystemC success stories featured at ICCAD, Japan Users Group Meeting**

SystemC Roadmap 2002-2003



Other OSCI activities – 2003-2004

- Evolve a synthesizable subset for behavioral synthesis and logic synthesis.
- Establish a firm standard for transaction level modeling (TLM).
 - Leverage current activities around Amba and OCPIP
- Examine ways to enhance SystemC for software modeling
- Encourage community growth and contribution

Real World Success With SystemC

- **Fujitsu: development & successful tape-out of a telecommunications SoC**
 - S/W modeling in SystemC + the new SoC design methodology
 - Cuts system-level-to-RTL design time by two-thirds!
- **ARM: Transaction Level Modeling (TLM) with SystemC**
 - Provides compelling answer to today's platform design challenges
 - Enables successful IP integration
- **Motorola: captured, verified & refined a system-level design from concept**
 - Executable functional spec to a ready-to-implement fully-specified architecture
 - Fast determination of commercial viability

Recent SystemC Stories in Japan

- Why have we chosen SystemC ?
 - Fumiaki Nagao
SANYO Electric Co.,Ltd.
- SoC system simulator development with SystemC
 - Kazuyoshi Takemura,
Matsushita Electric Industrial Co., Ltd.
- Key points to success valuable SoC design with SystemC
 - Hiroyasu Hasegawa,
H.D.Laboratories Co., Ltd.



Commercial Tool Momentum

- **New SystemC Products and Support from:**
 - Future Design Automation
 - Forte Design Systems – new Associate Corporate Member
 - Axys
 - Celoxica – new Associate Corporate Member
 - ChipVision
- **New SystemC Capabilities from:**
 - Synopsys
 - CoWare
 - Cadence
- **Look for companies with “Powered by SystemC” signs**

University Research

- See Booth #S6 for demos of:
 - OFFIS - Object-oriented SystemC Design
 - Uni Tübingen - SystemC Fixed-Point-Integer Conversion
 - TU Braunschweig - SDRAM Controller Simulation Environment
 - TU Chemnitz - SystemC Protocol Design
 - Uni Tübingen - Object-oriented SystemC Analysis and Synthesis, (OOAS Tool)
 - Uni Cantabria - SystemC Profiling Library
 - Uni Verona - LAERTE++ Testbench Environment

Summary

- Design challenges are moving up to the System Level
- SystemC provides critical capabilities for modeling, design and verification for HW/SW systems
- SystemC offers broad commercial tool support
- Join OSCI to help influence the future of System-level design at:

www.systemc.org