IP Integration-WG Update

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IP Integration Working Group

Group objectives

- Standardize the integration of IP verification models into the SystemC simulation environment
- Deliver tangible results Q2 2002
- Drive standardization via reference implementation
- Catalyst for standardization
  - Grow as we go, start with the easy specs first
  - Leverage verification model integration experience of participating companies

Who's in the WG

- IP
  - ARM
- Systems and Silicon
  - Fujitsu, Infineon, Motorola, STM
- Tools
  - Axys, Cadence, CoWare, Synopsys

Identified interfaces

- Bus model integration of IP
  - Peer-to-peer connection of bus interfaces
- HDL simulator integration
  - Using PLI or OMI
- SystemC as a slave
  - Integrating SystemC into foreign simulator

IP-WG current activities

- Jon Connell (ARM) leadership
- Focus is integration of IP with a transaction level bus model
  - Goal: an OSCI standard API for the integration of bus masters and bus slaves to transaction level bus implementations.
- Utilizing the Simple Bus Model (OSCI) framework identify additional requirements for the integration of verification models
  - Specify additions or modifications to the Simple Bus Model to satisfy these requirements
- Develop draft standard and reference implementation

Current status and plans

- Additional bus modeling requirements identified.
  - Requirements specification in-progress
- Functional Specification in-progress
  - Specification for Dynamic address decode done (ARM)
  - Specification for Address pipelining done (Synopsys)
- Complete Requirements specification April 2002
- Complete Functional specification June 2002

In-progress specifications

- Dynamic decode
  - Decoder to become a separate class (permit customization)
  - Methods added for mapping, remapping, aliasing, and lookup
- Address pipelining
  - Replace read/write transactions with phases: initiation (address+control), status, and data
    - Cycle-based
    - Most flexible interface scheme

Additional requirements

- Bus arbitration improvements
  - Ensure flexibility of arbiter interface for known arbitration schemes
- Address pipelining
- Dynamic decode
  - Allow slave remapping and aliasing
- Hierarchical bus structure
  - For example, Multi-layer AHB
- Split transactions
- Remove word-width restrictions & add 64 bit address
- Dual ported slaves