

SystemC Modelling of the X-Match Data Compressor for Multi-Gbit/s Networks

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Presentation Structure

- **Compression - Background**
- **X-Match Data Compressor**
- **Multi-X-Match Data Compressor**
- **Converting VHDL to SystemC**
- **Compiling SystemC code**
- **Verification of Design**

Compression - Background

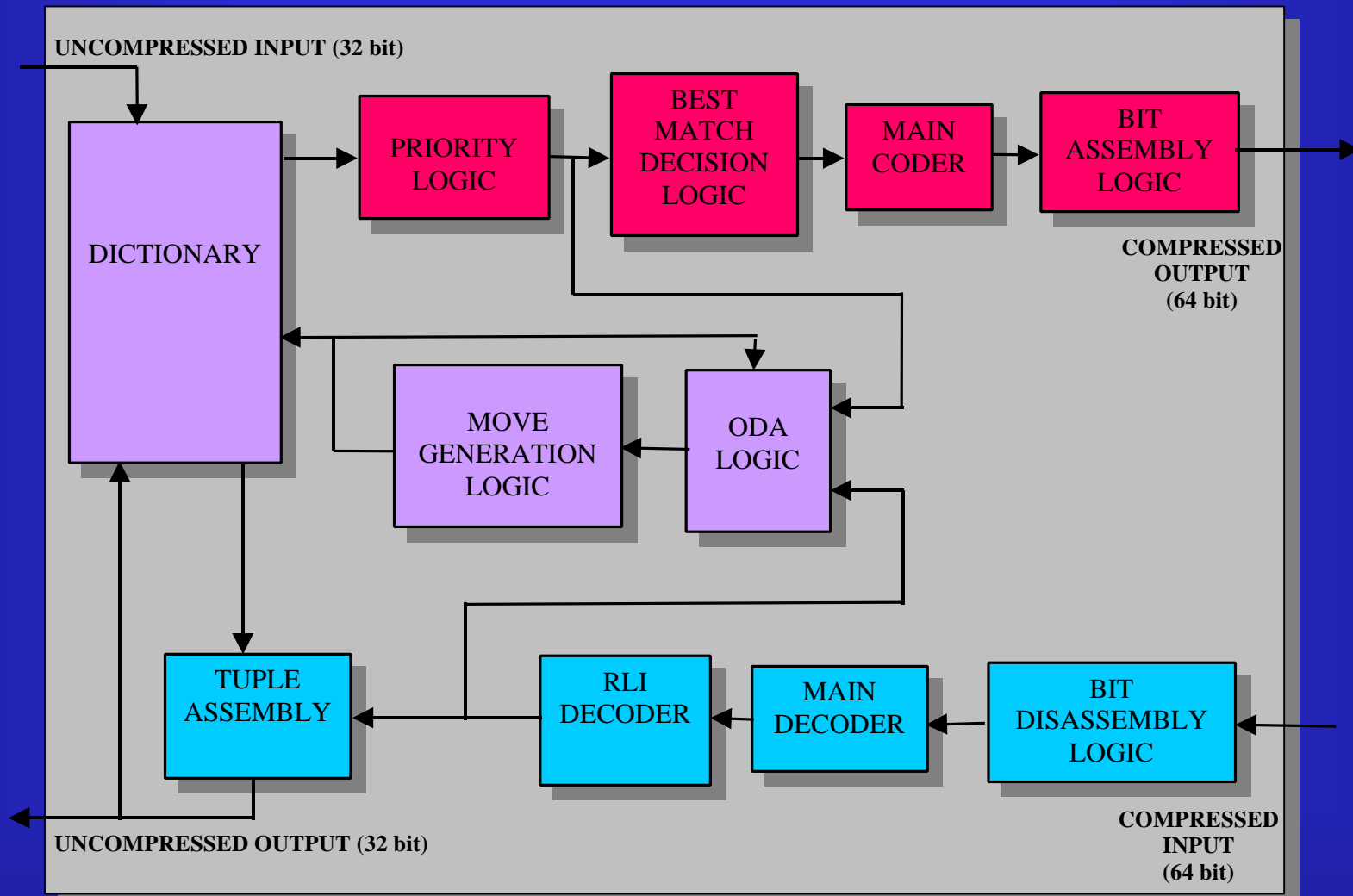
- **What is it ?**
 - **Identification and removal of redundancy from a piece of data**
- **Decompression**
 - **The reinsertion of some or all redundancy back into a piece of data**
- **Reduces bandwidth needed to transmit information**
 - **quicker or cheaper transmission**
- **Reduces physical storage volume of data**
 - **cheaper storage**

X-Match Data Compressor

High speed lossless data compressor/decompressor

- **SPEED** : 140MBytes/S
- **COMPRESSION** : 2:1
- **COMPLEXITY** : 100K gates for
128 word dictionary

Block Diagram of the X-Match Data Compressor

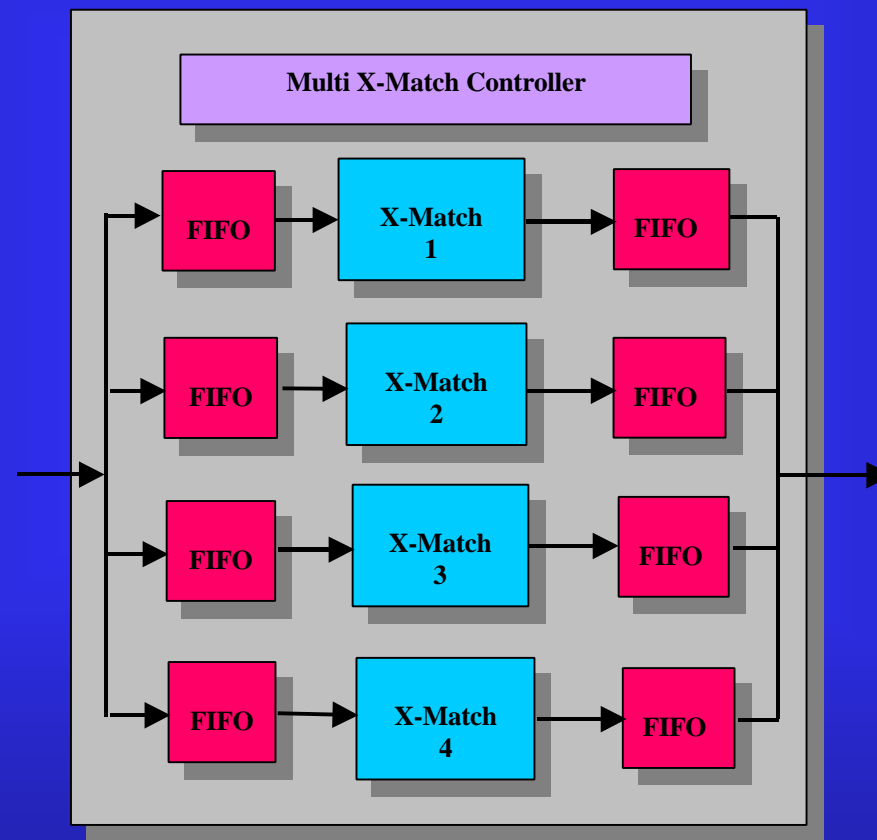


Multi-X-Match Data Compressor

Problem : Demand for Multi-Gbit/s networks meant present X-Match performance needs to be improved

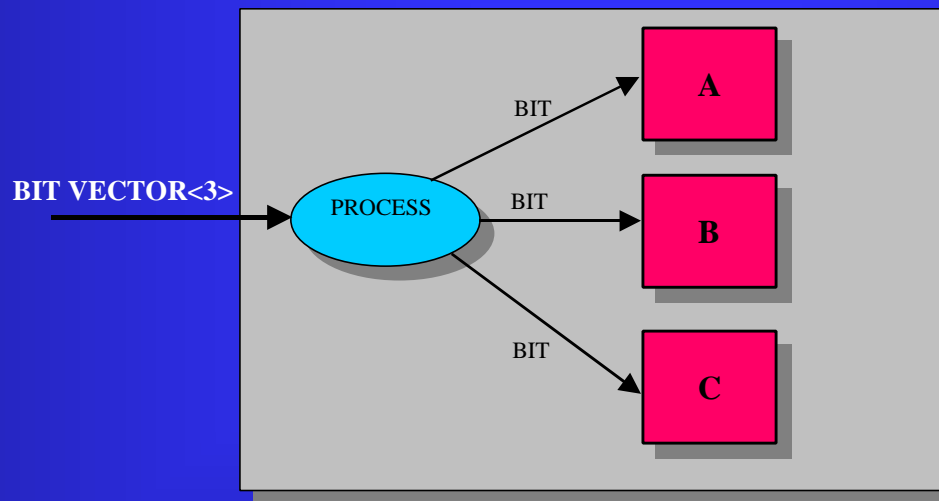
Proposed solution : A Multi-X-Match system with appropriate input and output data routing

Block Diagram of a Multi-X-Match System



VHDL to SystemC

- Straight forward conversion
Just different syntax used
- Bit selecting from an input signals



- The bit extraction operator '['] is defined for SystemC data types, but not for signals

Compiling SystemC Code

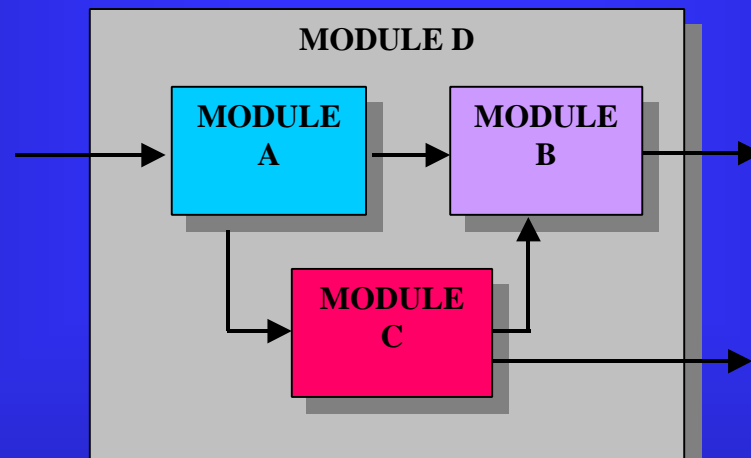
- **Cryptic error messages, such as**
(E1001) incompatible types for assignment :
- D:\SYSTEMC\SRC\sc_proxy.h: 993

**This error message is produced when assigning
bit/logic vectors of different lengths,**

- **SystemC Forum useful**
- **Examine source code can give additional
information.**
- **Look at sample code**

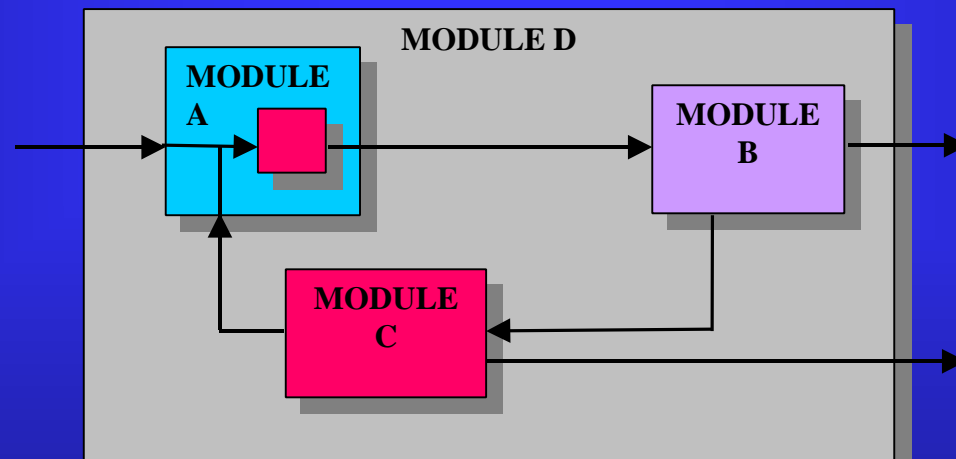
Verification of Design

- Bottom up approach verification



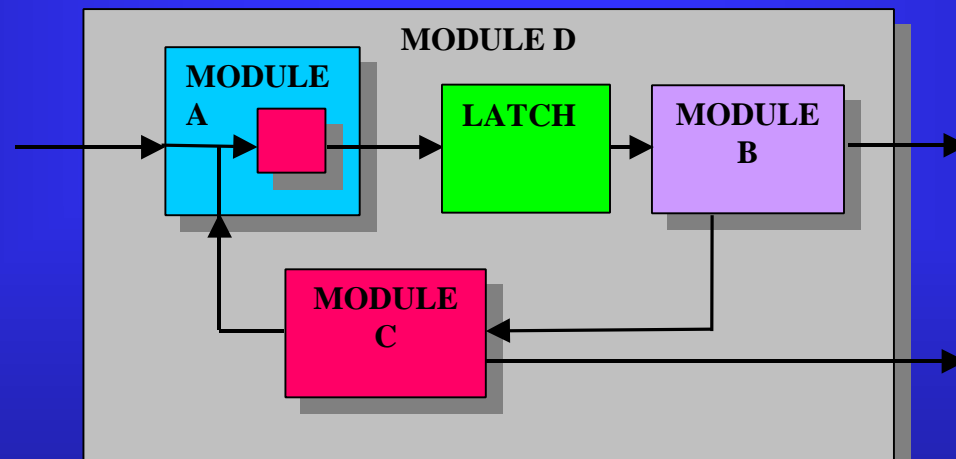
Verification of Design

Problem of signals updating each other (known systemc bug, fixed in later release). This causing the SystemC scheduler not to advance a clock cycle, unable to trace the waveform



Verification of Design

Solution involved placing a latch between various modules, breaking the continuous updating of signals and also helps determine which signals are causing the problems



Concluding Remarks

- All design information captured, simulated and verified
- Model suitable for being implemented into a larger system
- Resources which I found useful in learning SystemC are
 - SystemC Forum
 - Examining sample code
 - Documentation provided with files

Questions