
Specification of a PCI-compatible Interface for Telecom Systems

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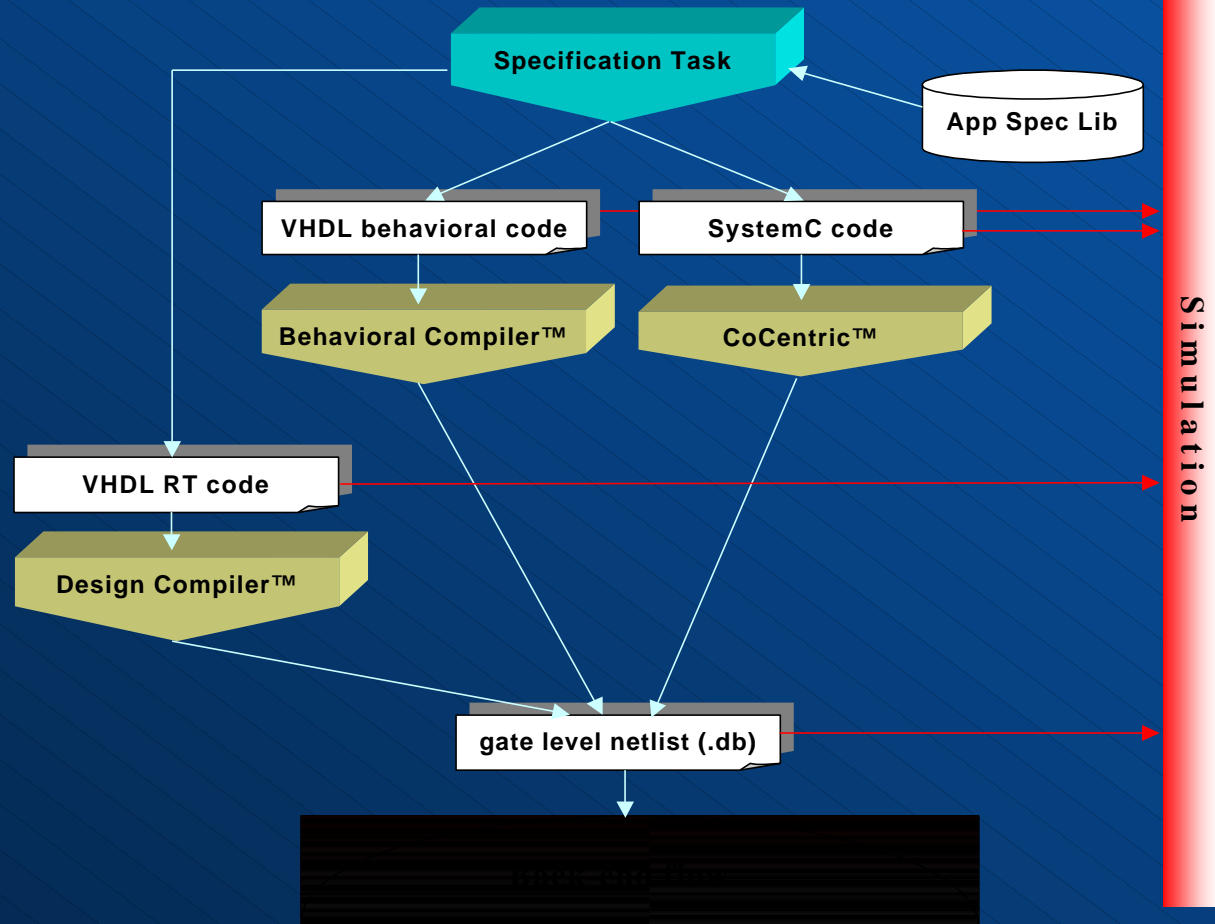
Summary

- ✓ Introduction
- ✓ Choice of SystemC for HW and System Design
- ✓ Industrial Design Flow and Methodology
- ✓ Customised PCI-interface
 - VHDL specification style
 - SystemC specification style
 - Comparisons between VHDL and SystemC Specifications
- ✓ Benefits of the current approach
- ✓ Conclusions and Future Works

SystemC for HW and System Design

- ✓ System level design capabilities
- ✓ Apt for mixed abstraction levels
- ✓ Real candidate for HW/SW developments
- ✓ Apt for SW development
- ✓ Apt for HW/SW interface descriptions
- ✓ Apt for RTL and behavioural level for HW development
- ✓ High potentialities for re-use
- ✓ Proposals for libraries developments in IST projects

Synthesis based design flow for SystemC



Modelling experiments in our design center

- ✓ RTL HW designs in Telecom domain (v. 1.0):
 - Data Processing Elements (DPEs)
 - Part of an MPEG decoder
 - Echo simulator (Reverberator)

- ✓ BUS interfaces (v. 1.x / v. 2.0):
 - Customised PCI-like interface for Base Station Controller
 - FPGA implementation for boards
 - Use of master/slave communication ports
 - Untimed abstract description of the application allowed
 - Channels/interface implementation left for v. 2.0

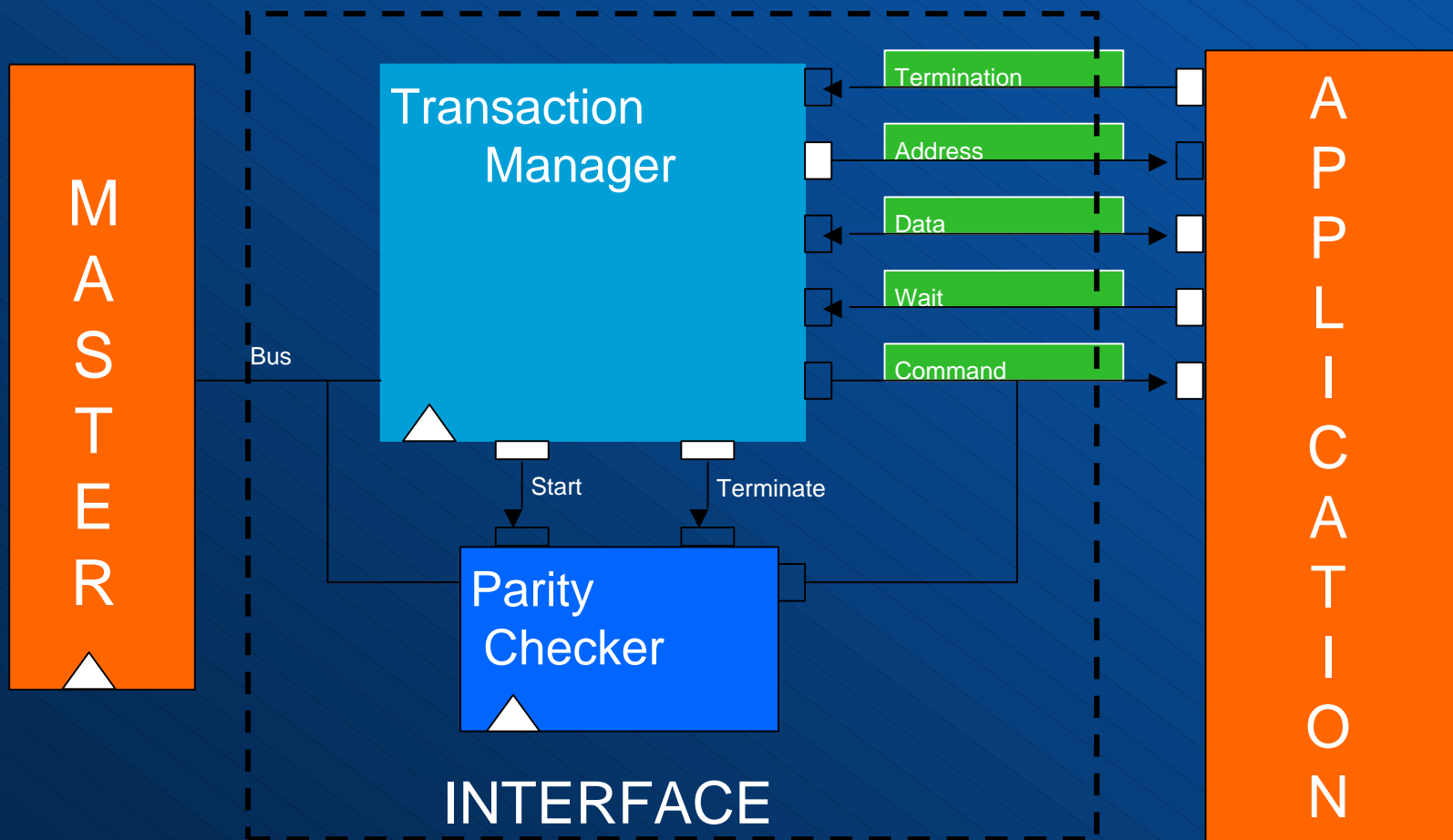
VHDL RTL Implementation

- ✓ Pure RTL description
 - FSM+DP architecture is not apt for this level of description
- ✓ Kernel functionalities identified
 - Bus transaction start controller
 - Address decoder
 - Data valid checker
- ✓ Each kernel functionality implemented as a process in the top architecture
- ✓ For synthesis tool reasons, reimplemented as components

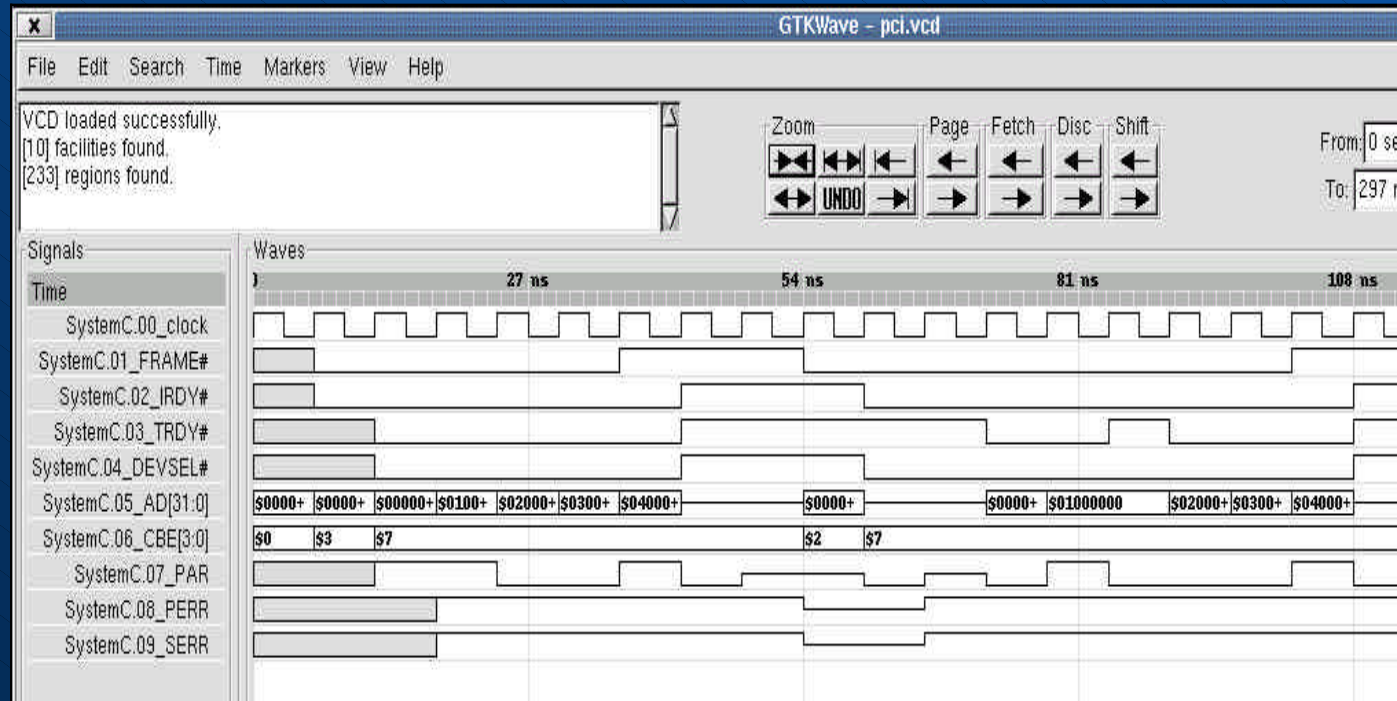
SystemC Implementation

- ✓ SystemC allows a more abstract description:
 - FSM architecture is the best for this level of description
- ✓ Two main functional blocks identified:
 - Transaction manager
 - Parity checker
- ✓ Test bench for validation:
 - stimuli generator acts as a transition master
 - standard SystemC kernel used
 - standard SystemC kernel signal monitor capabilities exploited
- ✓ The application using the interface modeled at an untimed level of abstraction

Structural Top Module Description



Multiple Data Phases Transaction Example



Feedback and benefits of the experience

- ✓ Ease of mixed abstraction design descriptions
 - encapsulation through the use of master/slave ports
 - planned interface channels usage will improve encapsulation capabilities
- ✓ Short learning time for designers with sw development background
- ✓ Ease of verification
 - due to untimed descriptions of the application
- ✓ VHDL/SystemC Simulation times are not comparable due to different abstraction levels
- ✓ All used tools are free on the net
- ✓ Modular project
 - encapsulation capabilities allowed easy task distribution

Conclusions and Future work

- ✓ Proved SystemC based flow in telecom domain
- ✓ Benefits for abstraction and reuse

- ✓ Need of application specific libraries
- ✓ Object Oriented methodological guidelines would be welcome

- ✓ Further steps will involve:
 - use of high-level synthesis tools
 - use of interface based design capabilities (v. 2.x)