



SystemC v2.0 Roadmap

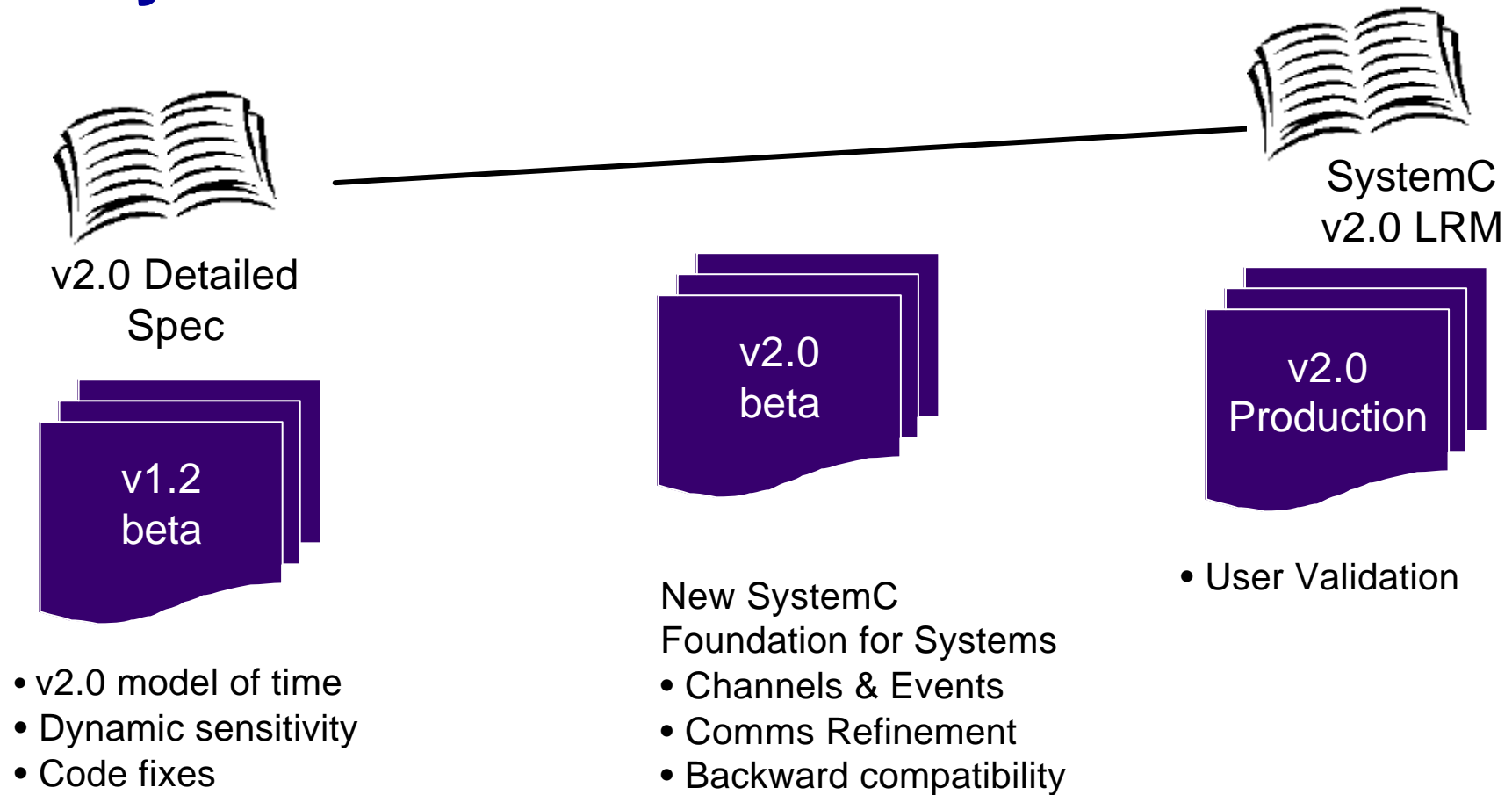
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SystemC v2.0 Innovation

- SystemC v1.0
 - RTL & behavioral level modeling (HDL & beyond)
 - integrated with higher level C/C++ functional modeling
- SystemC v2.0
 - provides higher levels of abstraction
 - enables modeling of HW / SW interaction
 - flexible communication channel refinement

SystemC Delivers



Feb
2001

Q2
2001

Q3
2001

SYSTEMC™

SystemC Release Roadmap

- 1.0 - Hardware Design Flow
 - RTL and Behavioral Hardware Modeling
- 1.x - Master-Slave Communication Library
 - RPC-based untimed & timed functional modeling down to RTL for bus protocol based systems
- 2.0 - System Design Flow
 - General purpose communication and synchronization
 - Communication Refinement
 - Multiple, customizable models of computation

SystemC Release Roadmap (cont)

- 2.X - Extensions to System Design Flow
 - Dynamic thread creation, fork / join
 - Interrupt / abort for behavioral hierarchy
 - Performance modeling support
 - Timing specification and constraints

- 3.X Software Design Flow
 - Abstract RTOS modeling
 - Scheduler modeling

- 4.X - Analog / Mixed Signal Systems Modeling