
System on Chip modeling with SystemC - Past and Future

SystemC Users Group Meeting

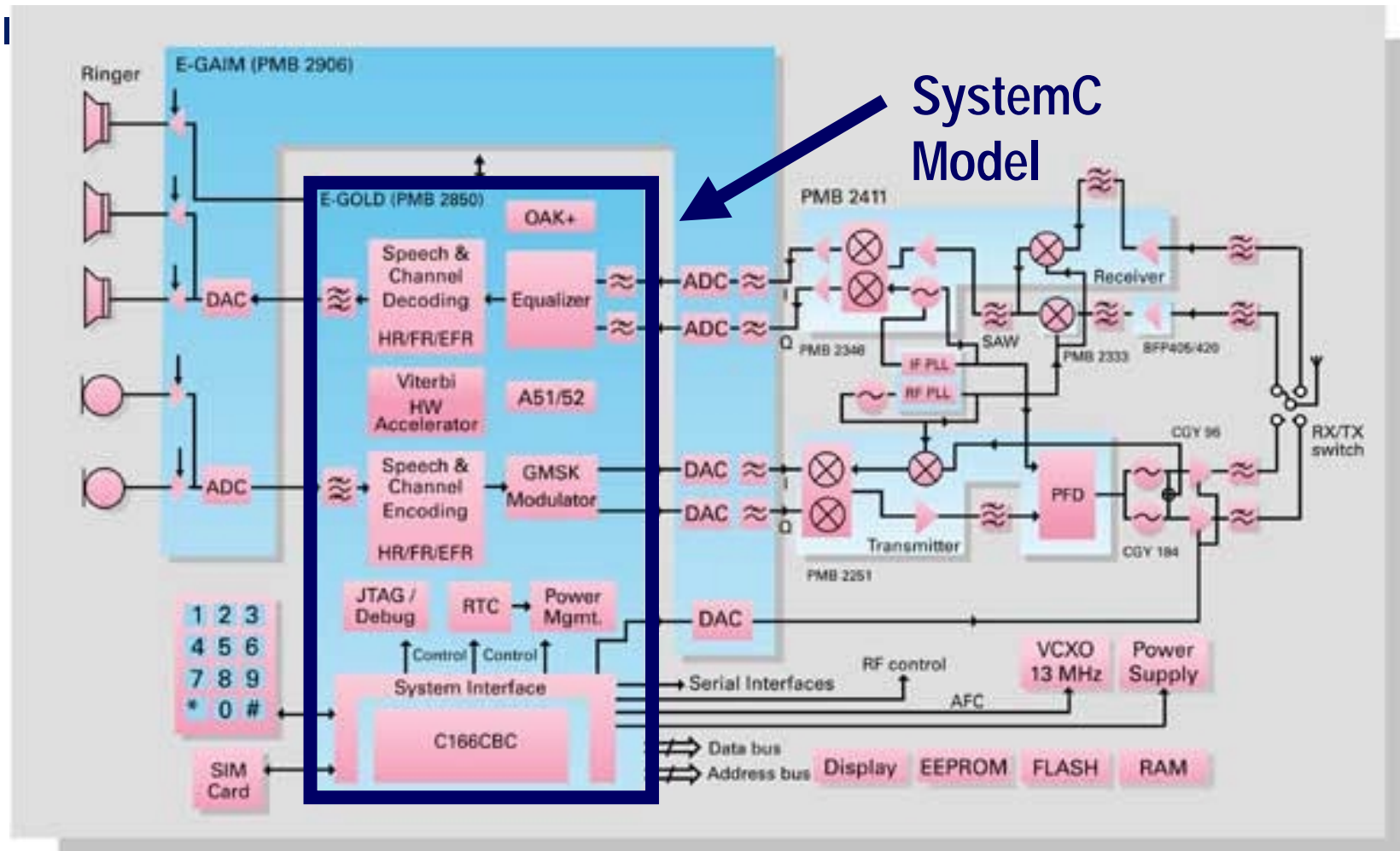
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System on Chip (SoC) Modeling with SystemC: The Past

- System hardware is modeled on block and signal (RTL) level.
- Software runs on simulated CPUs:
 - Instruction Set Simulator ISS with timing shell
 - Or cycle accurate CPU models
- Example: E-Gold GSM baseband chip

SystemC SoC Modeling Example : GSM Baseband Chip Set (E-Gold)



What's needed on Top for a System on Chip Development Platform

■ Simplicity

- No unnecessary details need to be considered
- “WYSIWYG” - what you see is what you get
 - Code is easy to understand
 - System behaves as expected
- Low entry effort, before the first system simulation runs

■ High simulation speed

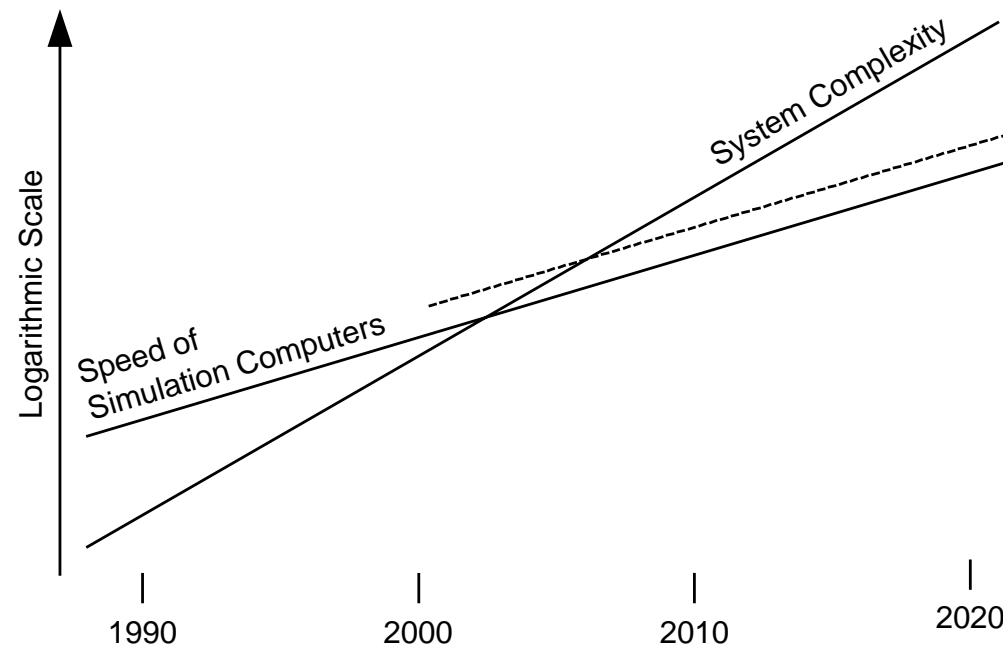
Required Simulation Speed grows exponentially due to System Complexity

- Size of systems on a chip grow by a factor of 4 every 3 years (“DRAM growth rule”).
- An optimistic estimation is, that a system with twice the size needs also twice as much functional evaluation and tests (doubled system simulation depth).
- A system with twice the size has half the simulation speed.

The system simulation performance requirements grow by more than a factor of 16 every 3 years or 160% per year.

Simulation Speed Requirements grow faster than the Performance of Simulation Computers.

- Speed of workstations increase by roughly 50% every year.
- C-Models (at same level as HDL) give a one time speed gain of up to one magnitude (parallel dotted line).



System Description with C++ is a Solution for the System Simulation Performance Challenge

- The only way to accelerate is a hierarchical simulation approach.
- Hierarchy starts at high level software. Hardware and “external world” are hidden for instance behind a driver API.
- If required, parts can be exchanged by more accurate (but slower) lower level models.
- This requires a modeling language (C++), which can be used across the whole modeling hierarchy, from high level software down to RTL hardware description.

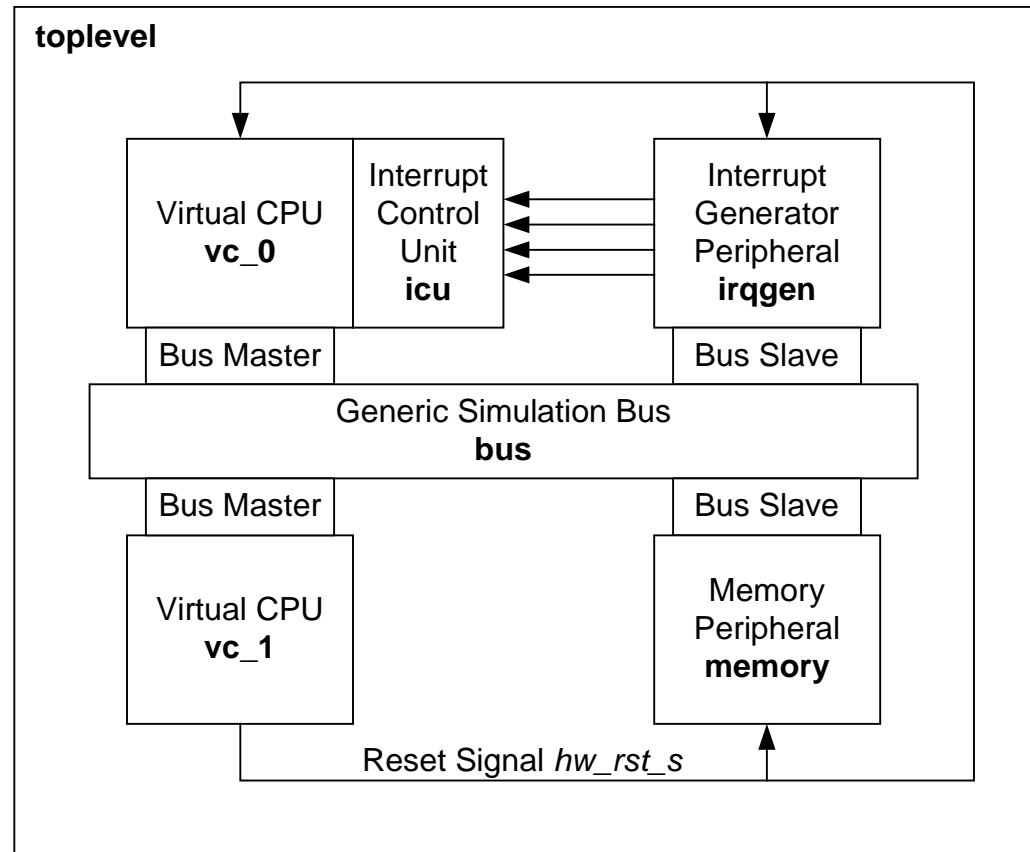
What's needed on Top for a System on Chip Development Platform

- Simplicity
- High simulation speed
- Several CPUs in one design
- One environment for hardware and software
 - One development and debug environment for hard- and software.
 - No border between software and hardware simulator
 - Support for hardware/software scenarios
 - Repository/archive for all parts of a simulation scenario
- Component Library
- Synthesis

System on Chip modeling: Future

- Scope: SoC modeling on architecture level, this means HW/SW partitioning done.
- SoC Platform comprising of:
 - Bus model
 - Bus masters and slaves
 - Methodologies representing the software part
 - Specific components (CPU, peripheral, memory models).
- SystemC V2.0 allows to model the bus on a higher abstraction level -> transactions.
- Standard components for busses, master and slave interfaces.
- The system is the testbench.

SystemC V2.0 like SoC modeling example IRQGEN Block Diagram



SystemC V2.0 like modeling SoC example IRQGEN Features

- Two CPUs, one peripheral and memory
- Transaction based bus and signals.
- IRQGEN specific code is 780 lines (including comment and empty lines)
- Integrated HW/SW environment and high speed due to Virtual CPUs. Virtual CPU base class provides:
 - Interfaces to other SoC components (clock, reset, bus, interrupts)
 - load() and store() methods.
 - Methods to register Interrupt Service Routines (ISR).
 - Reset output and reset response
 - Synchronization methods with testbench elements.

Summary

- SystemC has a solid basis to model accurately digital designs
- With SystemC V2.0 the right methods are available for more abstract architecture modeling
- Components with standard interfaces will be created on top of V2.0