

SystemC Impact on the Development of an IP Library

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CSELT PROPERTY

Vip libraryTM

Features

- **Synthesizable SOFT IP Library**
 - Parametric system-level modules (VHDL)
 - High degree of flexibility (generics)
 - Supplied with Testbench scenarios
 - Synthesis scripts (std cells, FPGAs)
- **Application areas**
 - Fast Packet Switching (ATM, IP Networking)
 - Multimedia
 - Wireless Communication

<http://www.csel.it/products/viplibrary>

Why SystemC for ICT Core Cells

- ICT products merge HW & SW
- System exploration (partitioning, co-simulation,...)
- Need for functional IP core models
- Ensure bit accuracy, cycle accuracy
- Explore architectures before RTL coding
- **SystemC meets these requirements!**
- Two directions in using SystemC
 - Preserve existing portfolio of IP cores
 - Introduce new design approaches

VHDL2SC Translator

- Requirements
 - Modeling at higher abstraction level of VIP Cores
 - Cycle accuracy/bit accuracy
- VHDL to SystemC translator
 - Based on V0.9 (started mid oct. '99)
 - Translates synthesizable VHDL (Synopsys DC-style)
 - Translated stmts & declarations
 - entity (code hiding through I/F function), architecture
 - generics (bit width, generate)
 - process
 - structural descriptions
 - 1D-2D array variables (signals in progress)
 - procedures, functions (even in packages)
 - enumerated data types

V2SC Workflow

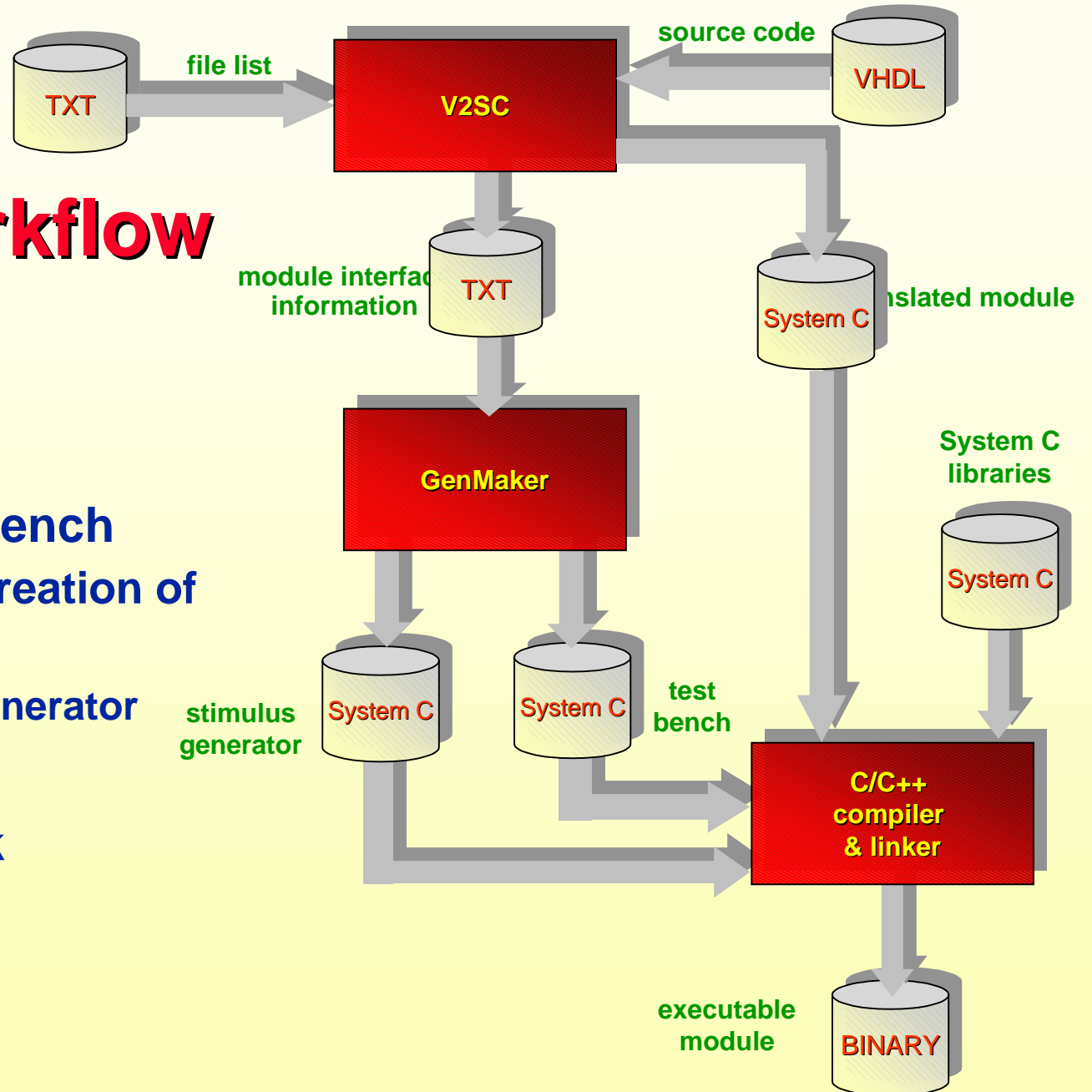
1 Translate

2 Generate Testbench

– Automatic Creation of

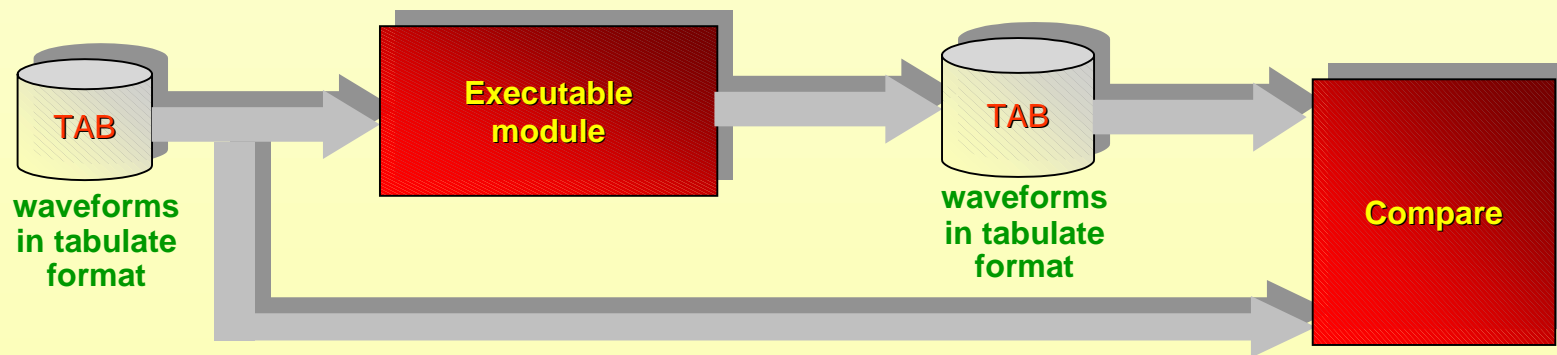
- Testbench
- Stimuli Generator

3 Compile & Link



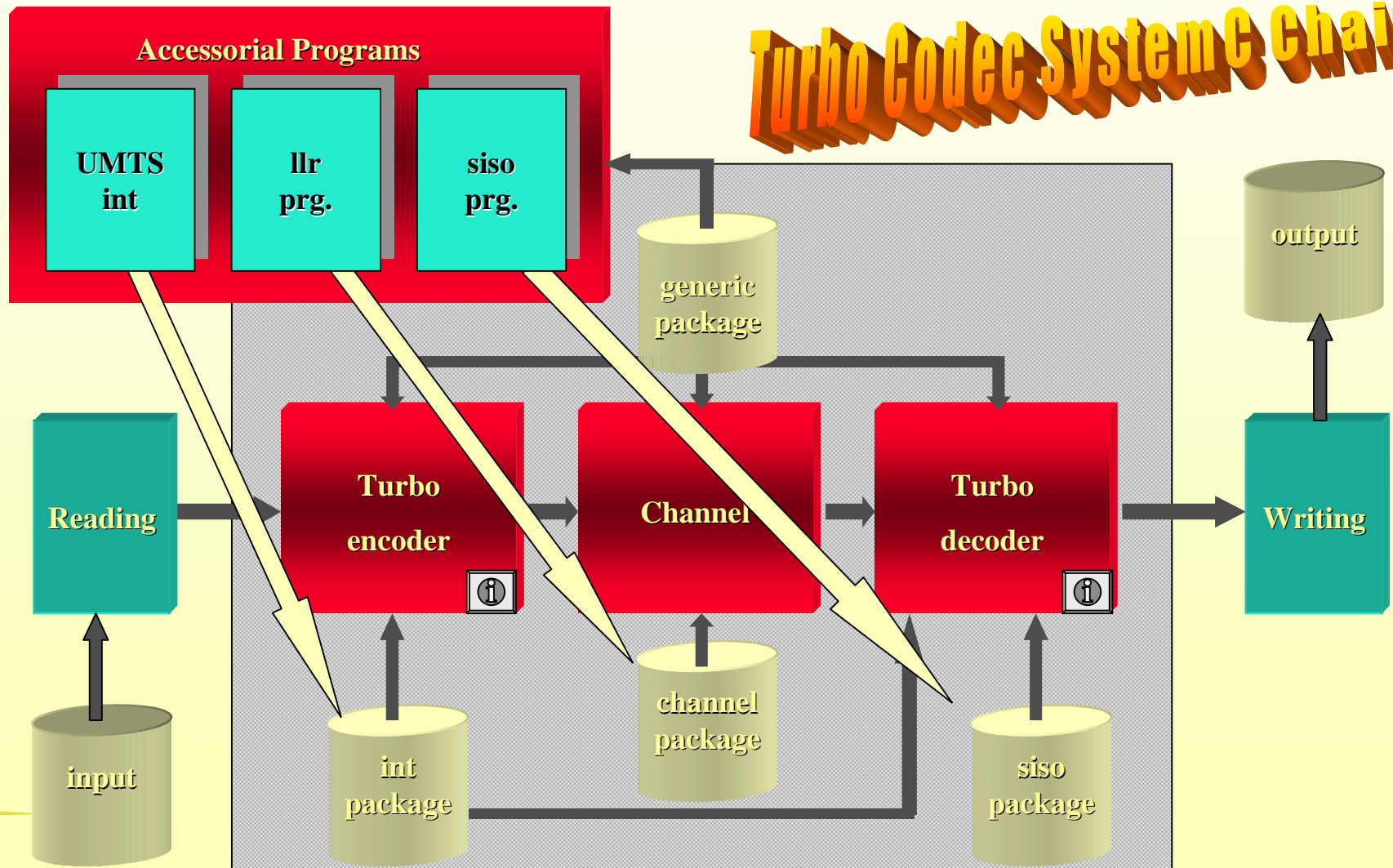
SystemC Simulation & Validation

- Input stimuli from VHDL simulation
- Model Accuracy
 - Cycle accuracy
 - Bit accuracy
- Easy comparison of Results
 - diff
 - cmp



New Design Approaches

Turbo Codec System C Chain



Conclusions

- **SystemC used to**
 - Create cycle/bit accurate models of IP cores
 - Perform architecture exploration
- **Issues in using SystemC**
 - v1.0 lost features to parameter passing
 - Initialisation of vectors with constant values in packages
 - Fixed point data types buggy (v1.0)
- **Future Perspectives**
 - HW/SW co-simulation for VIP library cores
 - SystemC synthesis to (V)HDL/gates
 - Top-down design methodology