Platform-driven ESL Design Solutions Update

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Three dimensions of ESL Design:

- **Product specification within its operating environment**
- **Path to hardware implementation**
- **Virtual hardware platform delivery for SW development**

“**System**” Environment around the Product
(Capture, Visualize, Utilize)

- **Product Specification**
  (“From grey-matter to bits”)
- **Path to Implementation**

Software (ESW)  Hardware (EDA)
Building High Performance Platforms

Platform-driven ESL Design

- Model the architecture and validate
- Model the functionality visible to SW
- Model HW for optimization & verification

Standards-based transaction-level modeling and reuse
Architects and Hardware designers use the same modeling methodology, simulation environment, and tools that are used to create the Virtual Platform for Software Development.
Creation of Virtual Platform does not require duplication of effort
Since the same model is used, it eliminates unintentional errors
Revisions to the hardware platform are delivered to the software team as soon as they are made
CoWare SystemC Solutions

CoWare Platform Architect

CoWare Model Library

SystemC Platform Capture and Analysis

CoWare Model Designer

SystemC IP Model Development and Debug
SystemC Modeling Library (SCML)

SCML is CoWare’s open SystemC Modeling Library API

- Defines a structured methodology for modeling SystemC TLM peripherals
- Built on top of IEEE, OSCI, and OCP SystemC and TLM standards

SCML combines with CoWare tools and IP to enable CoWare’s Platform-driven ESL Design solutions

- Enabling TLM peripheral model reuse across platform design tasks, levels of abstraction, and popular interconnect

Provides an easier way to learn SystemC TLM
Delivers higher re-use productivity
CoWare IP Model Library

- **Processors**
  - MIPS32 4Ke, MIPS32 24K, MIPS32 34K
  - ARM7/9/10/11 (11 CCM variants), IA models for ARM926, ARM968, ARM1136, and ARM1176 (all AHB and OCP), AMBA HWSW sc. lib.
  - ZSP 400 and ZSP 500
  - Toshiba MeP
  - CEVA TeakLite (II)
  - IBM PPC750GX/GL
  - Tensilica Xtensa, Tensilica Diamond Cores

- **Interconnects and bridges**
  - AMBA BL
  - AXI BL
  - Generic Multi-master OCP Bus
  - Sonics SMX

- **Peripherals**
  - AHB/APB PrimeCells
  - SCML based Generic IP Library (Library of 11)
  - SCML based Generic FRBM and Memory Controller

and more!
Algorithm and Accelerator Design

CoWare Processor Designer

CoWare Signal Processing Designer

- Extend application or modem performance with programmable accelerators
- Design advanced connectivity or modems for integration into advanced platforms
- Jump start your design and speed verification with proven reference library specifications

Optimizing performance for convergence products
Platform Distribution & Software Development

- Virtual Platform Generation from Platform Architect
  - TLM and SystemC
  - ESL methodology integration
  - Ultra fast ISS and SystemC Simulator
  - Packaging for distribution

- Virtual platform
  - Self contained software package
  - Controllability and observability tool
  - API and scripting

Synchronized HW/SW teams
Accelerated SW development
Supply chain enablement
CoWare ESL Ecosystem

EDA and FPGA
- Mentor Graphics
- Synplicity
- SYNOPSYS
- FORTE Design Systems
- EVE
- Tenison
- Nova
- Javelin
- ChipVision
- XILINX
- ACE
- Synfora
- Criticalblue
- X-FITTER
- Synopsys

ESW
- Cadence
- Green Hills Software
- Wind River
- ARM
- Montavista
- Eclipse
- Symbian
- Altia

IP
- VeriSilicon
- Synopsys
- ARM
- Cirrus Logic
- IBM
- Texas Instruments
- Texas Instruments
- CEVA
- SONICs
- Arteris
- Sistatix
- Tensilica
- Denali
- Synopsys
- ARC

Training
- Synopsys
- Mentor Graphics
- Synopsys
- X-FITTER
- Synopsys
- Synopsys
- Synopsys
- Synopsys
- Synopsys
- Synopsys

Services
- The MathWorks
- Texas Instruments
- DTDI
- HCL Technologies
- Newfield

Standards
- The SPIRIT Consortium
- OCP
- International Partnership
- SystemC
CoWare SystemC Solution Demos

- Multi-core embedded software development and debug
  - PDA Virtual Platform
  - Virtual platform packaging for distribution

- Multi-level hardware/software platform debug
  - Back-end Video Processing subsystem
  - CoWare Model Library

- Ask our experts about
  - Standards based SystemC TLM modeling methodology
  - Design flows with CoWare ecosystem partners
Thank you

Come see us at Booth R1
Rhodes Level 2