

Curriculum Vitae



Personal information

Title. Surname / First name(s) **Dr. Peranandam, Prakash Mohan**

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Date of birth 13-02-1977

Nationality Indian Gender : Male

Occupational field Formal Methods and System Verification

Type of business or sector Computer Science (PhD)

Area of Interest Formal & Functional verification of high level systems.
Semi formal verification techniques.
Functional verification process quality measurement.
Protocol modelling and verification.
Wireless communication and application.

Computer skills and competences

Software Development :
Formal Methods tools (Model Checking, BDD, Temporal logics)
Property verification tool enhancement and optimization
Symbolic traversal guiding tool
Transactional level verification tool
Transactional sequence coverage tool
Wireless communication - IP Convergence layer protocol (HiperLAN/2 Specification)
Membrane Computing – a Parallel system realization

Programming Languages :
Imperative language : C / C++, Java
Logic programming : Prolog
Design language : SystemC, VHDL
Modelling language : SDL
Verification language : e (Theoretical)
Property Spec. lang. : PSL
Various scripting language

Tools:
SymC : Symbolic bounded property verification tool
RAVEN : Real time model checker
SystemC checker : Simulation based property checking tool
GateProp : Formal property verification tool – CVE Property checking tool, Infineon AG.
Solidify : Static functional verification tool – Averant Inc.
SDL : Specification and Description Language – a Telelogic TAU SDL Suite
CVS : Version control system
CUDD : A Binary Decision Diagram (BDD) package
Semi formal tool : Academic semi formal methodology

Operating System:
Windows (NT, 2000, XP)
Unix (Linux, Solaris)

Work experience

Date	Occupation or position held	Main activities and responsibilities	Name and address of employer
Jan 2007 to till date	Post doctoral researcher	Functional verification quality measurement for designs – A collaborative project with Cadence, Munich, Germany.	University of Tuebingen, Tuebingen, Germany.
March 2003 to Dec 2006	Doctoral research candidate	Formal methods verification research and tool development. Also technical research paper reviews for conferences and workshops.	University of Tuebingen, Tuebingen, Germany.
March 2002 to March 2003	Commercial verification tool evaluation and book review	Formal verification tool evaluation for the firm Bosch, Reutlingen, Germany and review of SystemC book edited by W.M, W.R & J. Ruf.	University of Tuebingen, Tuebingen, Germany.
Oct. 2001 to Feb. 2002	Master thesis	Wireless communication protocol modelling with Quality of Service (QoS) and verification of the model.	Siemens, ICM MP TI 2, Bocholt, Germany.
May 2001 to Sep. 2001	Internship	Wireless communication protocol (HiperLAN/2 system) validation for European standard.	Siemens, ICM MP TI 2, C/o Bocholt, Germany
Sep. 2000 to Nov. 2000	part time job	Implementing part of the functionality in a e-shop project	Newtron AG, Dresden, Germany.

For more details on the listed items

please refer -- Annex - A

Education and training

Date	Title of qualification awarded	Principal subjects / occupational skills	Name and type of institute	Degree or Certification
March 2002 to Dec. 2006	Doctor rer. nat	Doctorate degree preparation on Formal methods Spec. + Verification	Uni. Tuebingen, Germany.	Doctorate degree (Dr. rer. nat.)
Oct. 1999 to Feb. 2002	Masters in computational logic	Logics, theorem proving, logic programming	TU Dresden, Germany.	Master degree (M.S)
Aug. 1998 to Nov. 1998	Training in Client / server application	Client / server application development	SIT institute, Chennai, India.	Certification course
Aug. 1994 to May 1998	Bachelor of Engineering in Computer Science	Computer science & Engineering, Mathematics, imperative programming and fundamental electronics	Kongu Engineering College, India.	Bachelor degree (B.E)

For more details on the listed items

please refer -- Annex - B

List of publications

1. Grid Based Fast Falsification For Bounded Property Checking
Forum on Design Languages (FDL), September 2007, Barcelona, Spain.
2. Fast Falsification Based on Symbolic Bounded Property Checking
43rd Design Automation Conference (DAC), July 2006, San Francisco, California, USA.
3. Overlap Reduction in Symbolic System Traversal
IEEE International High Level Design Validation and Test Workshop (HLDVT), November 2005, Napa valley, California, USA.
4. Distributed Symbolic Bounded Property Checking
Parallel and Distributed Methods in verification (PDMC), July 2005, Lisboa, Portugal.
5. Dynamic Guiding of Bounded Property Checking
IEEE International High Level Design Validation and Test Workshop (HLDVT), November 2004, sonoma valley, California, USA.
6. Transactional Level Verification and Coverage Metrics by means of Symbolic Simulation
GI/ITG/GMM Workshop, February 2004, Kaiserslautern, Germany.
7. Using Symbolic Simulation for Bounded Property Checking
Forum on Design Languages (FDL), September 2003, Frankfurt, Germany.
8. Bounded Property Checking with Symbolic Simulation
GI/ITG/GMM Workshop, February 2003, Bremen, Germany.
9. A Report: Computing with Membranes
<http://psystems.disco.unimib.it/>
10. Fast Distributed Property Checking (Poster)
UnivBooth: SystemC section DATE, March 2006, Munich, Germany.
11. Couple of technical and mile stone reports for project partners.

Personal skills and competences

Mother tongue

Tamil (Indian Language)

Other language(s) assessment

	Understanding		Speaking		Writing
	Listening	Reading	Spoken interaction	Spoken production	
English	Advanced proficient User	Advanced proficient User	Advanced proficient User	Advanced proficient User	Advanced proficient User
German	Basic User	Basic User	Basic User	Basic User	Basic User

Social skills & competences

Team spirit

Throughout my academic work, I was with various types of team and I proved to be productive and in general I enjoy the team environment that is very demanding.

Multicultural

I am quite adaptive and dynamic with multicultural environment, gained through my studies abroad and stay in student hostels and etc.

Communication

Over period of time, I gained excellent communication skills through presenting papers, discussions and talks among different groups and mingling with variety of people.

Representation

I represented Indian students in a Baden-Wuerttemberg state government (Germany) organized program for international students and obtained a certificate to represent Baden-Wuerttemberg for Indian students. I was also involved in discussion of "University study exhibition" in India organized by the same group.

Organizational skills & competences	<ol style="list-style-type: none"> 1. Co-chaired a session in a technical conference, FDL '03, September 2003, Frankfurt, Germany. 2. Supported some technical and conference arrangements during course of my PhD. 3. Gained confidence in organizing skills when I headed a first-aid group for a state level sports meet during my under graduate studies in India. 							
Research skills & competences	<ol style="list-style-type: none"> 1. Competent in problem solving and automation. 2. Efficient utilization of resources. 3. Good command in combining techniques in order to optimize and enhance efficiency. 4. Good and clear in promoting ideas by both written and oral. 5. Efficient in observing and learning the core content of ideas. 6. Productive at technical discussion. 7. Involved in university student project discussion – Bluetooth enabled intelligent wheelchair. 							
Driving License	Holding Indian and German driving license							
Hobbies	<ol style="list-style-type: none"> 1. Travelling, Music & Movies 2. Upgrading or assembling computers and fixing friend's computer related problems. 3. Personal electronic products. 4. Recent winter hobby: Improving my Skiing ability. 							
Additional information	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td data-bbox="300 902 438 936" style="width: 30%; vertical-align: top;">References :</td> <td data-bbox="515 824 1010 1025" style="width: 35%; vertical-align: top;"> Prof. Wolfgang Rosenstiel, Sand 13, Wilhelm-Schickard-Institut für informatik University of Tuebingen, 72076 Tuebingen, Germany. email : rosenstiel@informatik.uni-tuebingen.de phone : 0049 (0) 7071 29 75 482 </td> <td data-bbox="1082 824 1497 969" style="width: 35%; vertical-align: top;"> Dr. Juergen Ruf, IBM Deutschland, 71032 Boeblingen, Germany. email : jruf@de.ibm.com phone : 0049 (0) 7031 16 19 25 </td> </tr> <tr> <td></td> <td data-bbox="515 1048 1010 1249" style="vertical-align: top;"> Dr. Thomas Kropf Sand 13, University of Tuebingen, 72076 Tuebingen, Germany. email : kropf@informatik.uni-tuebingen.de phone : 0049 (0) 7071 29 75 482 </td> <td data-bbox="1082 1048 1497 1216" style="vertical-align: top;"> Mr. Wolfgang Groeting, BenQ Mobile, Neutorplatz 3-4 46395 Bocholt, Germany email : wolfgang.groeting@siemens.com phone : 0049 (0) 2842 95 2142 </td> </tr> </table>		References :	Prof. Wolfgang Rosenstiel, Sand 13, Wilhelm-Schickard-Institut für informatik University of Tuebingen, 72076 Tuebingen, Germany. email : rosenstiel@informatik.uni-tuebingen.de phone : 0049 (0) 7071 29 75 482	Dr. Juergen Ruf, IBM Deutschland, 71032 Boeblingen, Germany. email : jruf@de.ibm.com phone : 0049 (0) 7031 16 19 25		Dr. Thomas Kropf Sand 13, University of Tuebingen, 72076 Tuebingen, Germany. email : kropf@informatik.uni-tuebingen.de phone : 0049 (0) 7071 29 75 482	Mr. Wolfgang Groeting, BenQ Mobile, Neutorplatz 3-4 46395 Bocholt, Germany email : wolfgang.groeting@siemens.com phone : 0049 (0) 2842 95 2142
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	Dr. Thomas Kropf Sand 13, University of Tuebingen, 72076 Tuebingen, Germany. email : kropf@informatik.uni-tuebingen.de phone : 0049 (0) 7071 29 75 482	Mr. Wolfgang Groeting, BenQ Mobile, Neutorplatz 3-4 46395 Bocholt, Germany email : wolfgang.groeting@siemens.com phone : 0049 (0) 2842 95 2142						

Annex – A

Work Experience

Jan 2007 to till date	
Responsibilities & Experience	<p>Post Doctoral Researcher at Formal Methods Group, University of Tuebingen, Germany.</p> <p>Researching to develop a strategy & methodology to measure the quality of functional verification process. This measurement in turn can then be applied to calculate the whole productivity of a whole system. This research project is taken over and partitioned among multiple firms like Bosch, Cadence, Infineon, AMD and some universities.</p> <p>Main work includes : Functional verification Quality Modelling & Fuzzy logic based static quality measurement</p>
Employer Details	<p>Prof. Dr. Wolfgang Rosenstiel, University of Tuebingen, Sand 13, 72076 Tuebingen, Germany.</p>
March 2003 to Dec. 2006	
Responsibilities & Experience	<p>Doctoral candidate & Formal Methods Group research staff.</p> <p>Evaluated commercial formal hardware verification tools for the firm Bosch</p> <p>Designing the verification plans for a given hardware</p> <p>Involved in academic project to develop and optimize formal hardware verification tools using C/C++.</p> <p>Guided couple of students in their student projects.</p> <p>Project reports and academic research paper writing</p> <p>Research discussions and new heuristic development for hardware verification</p> <p>Delivering speech and presenting the academic research work in meetings and international conferences</p> <p>Evaluation of research papers for conferences and technical reviews for books and workshops.</p>
Employer Details	<p>Prof. Dr. Wolfgang Rosenstiel, University of Tuebingen, Sand 13, 72076 Tuebingen, Germany.</p>
March 2002 to Mar. 2003	
Responsibilities & Experience	<p>Formal Methods Group research staff.</p> <p>Commercial formal verification tool evaluation for the firm Bosch, Reutlingen, Germany, for their use as a part of the collaborative project. Additionally, doctoral degree preparatory work and technical review for a book and papers.</p>
Employer Details	<p>Prof. Dr. Wolfgang Rosenstiel, University of Tuebingen, Sand 13, 72076 Tuebingen, Germany.</p>
Oct 2001 to Feb 2002	
Responsibilities & Experience	<p>Master thesis student</p> <p>Implemented the IP convergence layer with Quality of Service Support.</p> <p>Validated the IP convergence layer concept using π- calculus</p> <p>Expertise the modelling language "Specification and Description Language" (SDL)</p> <p>Project development discussions</p> <p>Technical writing</p>
Employer Details	<p>Mr. Wolfgang Groeting, Siemens, ICM MP T1 2, Neutorplatz 3-4, 46395 Bocholt, Germany.</p>

Annex – A Cont.

May 2001 to Sep 2001

Employer Siemens, ICM MP TI 2, Bocholt, Germany.

Position Internship student

Responsibilities & Experience Validated the HiperLAN/2 system protocol for European standard
Mastered the modelling language "Specification and Description Language" (SDL)
Gained the industrial work experience and work environment

Employer Details Mr. Wolfgang Groeting, Neutorplatz 3-4, 46395 Bocholt, Germany.

Sep 2000 to Nov 2000

Employer Newtron AG, Freiburgerstrasse 39, 01067 Dresden, Germany.

Position Part time programming job

Responsibilities & Experience Implemented the part of the functionality in e-shop project.
Experienced the java programming
Understood and used the version repository system
Team work

Employer Details T. Jacobi, Newtron AG, Freiburgerstrasse 39, 01067 Dresden, Germany.

Annex – B

Education & Training

March 2002 to Dec 2006

Title of Qualification awarded

Doctorate in Computer Science

Principal subject

Formal verification method (model checking, symbolic simulation)
Semi formal verification (combined approach, Local model checking)
Functionality coverage metrics
Symbolic guided traversal

occupational skills covered

Functional verification (simulation based approaches)
Assertion based verification
Verification related fields(Functionality & code coverage, system design)
Software verification
Involved in academic project to develop and optimize formal hardware verification tools using C/C++.
Guided couple of students in their student projects.
Project reports and academic research paper writing
Research discussions and new heuristic development for hardware verification
Delivering speech and presenting the academic research work in meetings and international conferences
Evaluation of research papers for conferences and workshops

Thesis Abstract:

My PhD thesis is about intelligent heuristics that optimizes and increases the efficiency of the Divide-and-Conquer approach of the symbolic state space traversal based property verification tool. The major contributions are two heuristics, first *MinOverlap* algorithm for the full validation approach and the other is *Guiding* algorithm for the fast falsification approach.

The *MinOverlap* algorithm aims at reduction of state overlap of different partitions that eventually minimizes the redundant computation and decreases the verification time. The *Guiding* algorithm aims at automatic steering the state space traversal in the direction of the errors and avoids the uninteresting state space, saving the memory and fast finding of bugs.

The heuristics can be efficiently applied in full validation and fast falsification approaches of both "*Splitting*" and "*Windowing*" techniques of the formal verification. *MinOverlap* algorithm exploits the design's transition relation and forms the influence table for all the state variables as a pre-processing step. This influence information is then utilized while state space partitioning for an interesting set of variables. The *Guiding* algorithm utilizes the transition relation of the design along with the information of the property to be verified in order to find the set of interesting variables to guide and steer the traversal towards the bug.

Annex – B Cont.

Oct 1999 to Feb 2002

Title of Qualification awarded

Masters in Computational Logic / German Diplom Informatiker

Principal subject

Computational Logics, Structural proof theory
Multi-agent systems, Logic programming
 π – Calculus, Formal Software development
Formal specification of software systems.

occupational skills covered

Natural language processing
Clustering methods for Data mining and analysis
Prolog programming
Membrane computing
Seminar and group discussion

Aug 1998 to Nov 1998

Title of Qualification awarded

Certificate of client / server application

Principal subject

Client server technology based programming

occupational skills covered

Visual Basic programming with MS Access and SQL

Aug 1994 to May 1998

Title of Qualification awarded

Bachelor of Engineering in Computer Science

Principal subject

Introduction to Computer science
Imperative programming language
Data base
Compiler design,
Computer Networks
Digital logics and circuits
Electrical and Electronic Engineering

occupational skills covered

General concepts of computer science
Imperative language programming